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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,338	02/28/2002	Yukikazu Matsuo	50090-478	5606

7590 07/02/2004

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/02/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,338	MATSUO ET AL.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *1-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are pending and are hereby presented for examination.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "pseudo bypass register" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The specification is objected to under 37 CFR 1.71 because the specification lacks an enabling description for claims 1-8, in reference to limitation "pseudo bypass register".

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title does not adequately describe the claimed invention. The following title is suggested: Testing device and test mode for semiconductor integrated circuit having pseudo bypass registers.

Appropriate correction is required.

Claim Objections

5. Claim 1-5 are objected to because of the following informalities:

Claim 1, line 4, a comma or colon should be inserted after the transitional parse "wherein". Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to properly define the function of a "pseudo bypass register" recited in the independent claim 1, 6 and 7. The specification, in the summary of the invention, describes "a pseudo bypass register having a bypassing function of the test data input" which is not adequate to enable a person skilled in the art to make use of the claimed invention.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4 and 5 recite: " whereby ...." Such recitation is non-functional language, and as a result, is not given patentable weight. It has been held that functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish in re Mason, 114 USPQ, 44 CCPA 937 (1957).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawano et al. (US 5781560).

Regarding independent Claims 1, 6 and 7, Kawano substantially discloses a system and method for testing a semiconductor integrated circuit (LSI 1-LSI n) equipped with logic circuits and JTAG circuits (601-1-601-n) FIG. 7. In view of claims rejection under 35 U.S.C. 112, first paragraph, for examination purpose, the Examiner interprets the "pseudo bypass register" to mean "a bypass register".

The JTAG circuit, FIG. 8, includes:

A boundary scan register (701) that executes a test of the logic circuits inside (LSI 1-LSI n) in accordance with a test data input (DTI) and stores a test result from the logic circuits, a data register (704) and a first selector MUX 3 (706) connected to the data register (704), which selectively takes out outputs of the registers.

A bypass register (702) having a bypassing function of the test data input TDO by enabling the test data input TDI to be bypassed to the test data output TDO, an instruction register (707) for giving an operation command and a second selector MUX 4 (703) that is connected to the boundary scan register (701), the first selector MUX 3 (706), the bypass register (702), and the instruction register (707), which is selectively controlled by the instruction register.

JTAG circuits (601-1-601-n) provided to each of the logic circuits associated with each (LSI 1-LSI n), where the test data output TDO of the JTAG circuit of the LSI 1 is connected to the test data input TDI of the JTAG circuit of the LSI 2, FIG. 7.

Regarding claims 1-6 and 7, Kawano does not explicitly disclose a pseudo bypass register having a bypassing function of the test data input, wherein the pseudo bypass register is controlled by the data register selecting the first selector, has the same configuration as that of the bypass register, has a selector provided on the input thereof, where the test data input to be bypassed and arbitrary information can be inputted selectively and by each bit.

However, Kawano discloses bypass register 102, which is used when data are bypassed from a JTAG circuit to another JTAG circuit, by enabling the test data input TDI to be bypassed to the test data output TDO. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the bypass register as taught by Kawano, since the bypass register performs the identical function of a pseudo bypass register, thus being cost effective by avoiding adding another register.

Regarding Claim 8, Kawano discloses a test method of a semiconductor integrated circuit (LSI 1-LSI n), which is used by in-circuit test JTAG circuits (601-1-601-n) for testing the logic circuits corresponding to (LSI 1-LSI n).

Conclusion

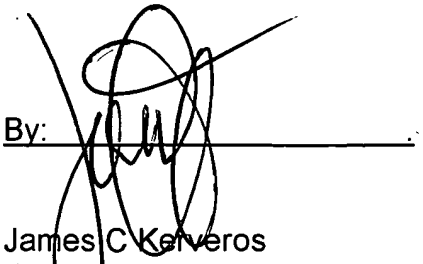
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 24 June 2004
Office Action: Non-Final Rejection

By: 

James C Kerveros
Examiner
Art Unit 2133

Guy J. Lamarre
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Primary Examiner